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A Versatile Control Scheme For Dynamic Voltage Restorer To Limit Downstream Fault Currents

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Abstract—
The Dynamic Voltage Restorer (DVR) is a custom power device utilized to counteract voltage sags. It injects controlled three-phase ac voltages in series with the supply voltage, subsequent to voltage sag, to enhance voltage quality by adjusting the voltage magnitude, wave shape, and phase angle. The DVR is conventionally bypassed during a downstream fault to prevent potential adverse impacts on the fault and to protect the DVR components against the fault current. This paper proposes an augmented control strategy for the DVR that provides:1) voltage-sag compensation under balanced and unbalanced conditions and 2) a fault current interruption (FCI) function. This paper introduces and evaluates an auxiliary control strategy for downstream fault current interruption in a radial distribution line by means of a dynamic voltage restorer (DVR). The proposed controller supplements the voltage-sag compensation control of the DVR. It does not require phase-locked loop and independently controls the magnitude and phase angle of the injected voltage for each phase. Fast least error squares digital filters are used to estimate the magnitude and phase of the measured voltages and effectively reduce the impacts of noise, harmonics, and disturbances on the estimated phasor parameters, and this enables effective fault current interrupting even under arcing fault conditions. The performance of the DVR for fault current interruption is analyzed by using MATLAB/SIMULINK software.

Index Terms—Digital filters, dynamic voltage restorer (DVR), fault current interrupting, and multiloop control.

I. INTRODUCTION

The Dynamic voltage restorer (DVR) is a custom power device utilized to counteract voltage sags. It injects controlled three-phase ac voltages in series with the supply voltage, subsequent to voltage sag, to enhance voltage quality by adjusting the voltage magnitude, wave shape, and phase angle. Fig. 1 shows the main components of a DVR (i.e., a series transformer, a voltage- source converter (VSC), a harmonic filter, a dc-side capacitor, and an energy storage device). The line-side harmonic filter consists of the leakage inductance of the series transformer and the filter capacitor. The DVR is conventionally bypassed during a downstream fault to prevent potential adverse impacts on the fault and to protect the DVR components against the fault current.

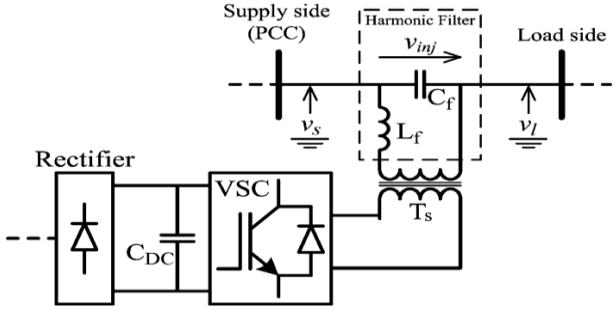

Fig. 1. Schematic diagram of a DVR with a line-side harmonic filter.

A technically elaborate approach to more efficient utilization of the DVR is to equip it with additional controls and enable it also to limit or interrupt the downstream fault currents. The main drawback of this approach is that the dc-link voltage of the DVR increases due to real power absorption during fault current-limiting operation and necessitates a switch to bypass the DVR when the protective relays, depending on the fault conditions, do not rapidly clear the fault. The dc-link voltage increase can be mitigated at the cost of a slow-decaying dc fault current component using the

methods introduced in. To overcome the aforementioned limitations, this paper proposes an augmented control strategy for the DVR that provides: 1) voltage-sag compensation under balanced and unbalanced conditions and 2) a fault current interruption (FCI) function. The former function has been presented in and the latter is described in this paper. It should be noted that limiting the fault current by the DVR disables the main and the backup protection (e.g., the distance and the over current relays). This can result in prolonging the fault duration. Thus, the DVR is preferred to reduce the fault current to zero and interrupt it and send a trip signal to the upstream relay or the circuit breaker (CB). It should be noted that the FCI function requires 100% voltage injection capability. Thus, the power ratings of the series transformer and the VSC would be about three times those of a conventional DVR with about 30%–40% voltage injection capability. This leads to a more expensive DVR system. Economic feasibility of such a DVR system depends on the importance of the sensitive load protected by the DVR and the cost of the DVR itself. The performance of the proposed control scheme is evaluated through various simulation studies in the Matlab/Simulink platform. The study results indicate that the proposed control strategy: 1) limits the fault current to less than the nominal load current and restores the PCC voltage within less than 10 ms, and interrupts the fault current within two cycles; 2) it can be used in four- and three-wired distribution systems, and single-phase configurations; 3) does not require phase-locked loops; 4) is not sensitive to noise, harmonics, and disturbances and provides effective fault current interruption even under arcing fault conditions; and 5) can interrupt the downstream fault current under low dc-link voltage conditions.

II. PROPOSED FCI CONTROL STRATEGY

The adopted DVR converter is comprised of three independent H-bridge VSCs that are connected to a common dc-link capacitor. These VSCs are series connected to the supply grid, each through a single-phase transformer. The proposed FCI control system consists of three independent and identical controller's one for each single-phase VSC of the DVR. The FCI function requires a phasor parameter estimator (digital filter) which attenuates the harmonic contents of the measured signal. To attenuate all harmonics, the filter must have a full-cycle data window length which leads to one cycle delay in the DVR response. Thus, a compromise between the voltage injection speed and disturbance attenuation is made. The designed
LES filters utilize a data window length of 50 samples at the sampling rate of 10 kHz and, hence, estimate the voltage phasor parameters in 5ms. Fig. 2 depicts the frequency response of the LES filters and indicates significant attenuation of voltage noise, harmonics, and distortions at frequencies higher than 200 Hz and lower than 50 Hz. Reference demonstrates the effectiveness of this filter in attenuating the noise, harmonics, and distortions for the sag compensation mode of operation as well. The next section shows that this filter also performs satisfactorily in the FCI operation mode, even under arcing fault conditions where the measured voltage and current signals are highly distorted. The proposed multi loop control system includes an outer control loop (voltage phasor control) and an inner control loop (instantaneous voltage control).

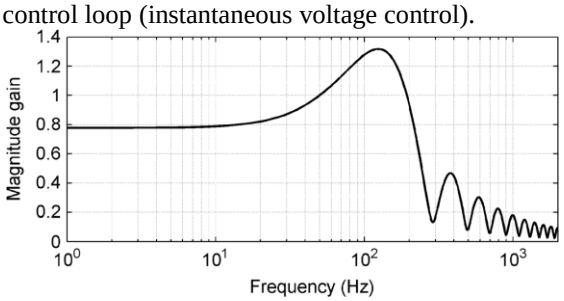

Fig. 2. Magnitude of the LES filters frequency response.

The inner loop provides damping for the transients caused by the DVR harmonic filter and improves the dynamic response and stability of the DVR. The inner loop is shared by the sag compensation and the FCI functions. When a downstream fault is detected, the outer loop controls the injected voltage magnitude and phase angle of the faulty phase(s) and reduces the load-side voltage to zero, to interrupt the fault current and restore the PCC voltage. The DVR "outer" voltage phasor control and "inner" instantaneous voltage control, corresponding to each phase, are described in the following two subsections.

III. STUDY RESULTS

Fig. 3 depicts a single-line diagram of a power system which is used to evaluate the performance of the proposed DVR control system under different fault scenarios, in the Matlab/Simulink software environment. A 525-kVA DVR system is installed on the 0.4-kV feeder, to protect a 500-kVA, 0.90 lagging power factor load against voltage sags.

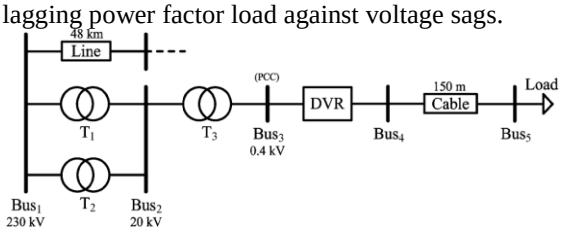

Fig.3. Single-line diagram of the system used for simulation studies.

Parameters of the simulated power system and the DVR are given in Appendix A. In the reported studies, the base voltage for per-unit values is the nominal phase voltage. Besides, voltage and current waveforms of phases A, B, and C are plotted by solid, dashes, and dotted lines, respectively.

A. Three-Phase Downstream Fault

The system is subjected to a three-phase short circuit with a negligible fault resistance at 20 ms at bus5. Prior to the fault inception, the DVR is inactive (in standby mode) (i.e., the primary windings of the series transformers are shorted by the DVR). During the fault if the DVR is bypassed, the voltage at Bus3 drops to 0.77 p.u. and the fault current increases to about 17 times the rated load current.

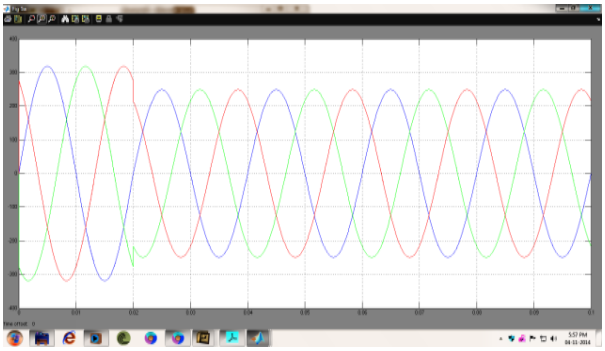

Fig. 4 (a) Voltages at bus3.

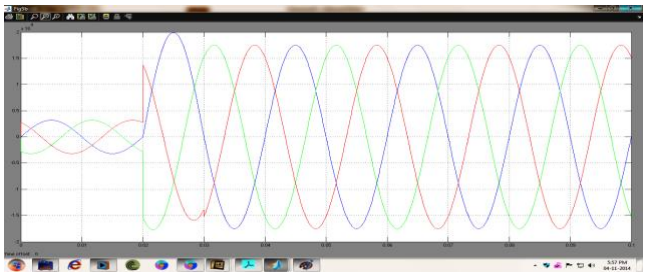

Fig. 4(b) Fault currents, during downstream three-phase fault when the DVR is inactive (bypassed).

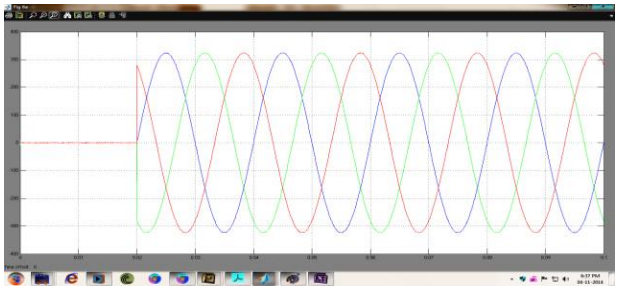

Fig. 5 (a) Injected voltages.

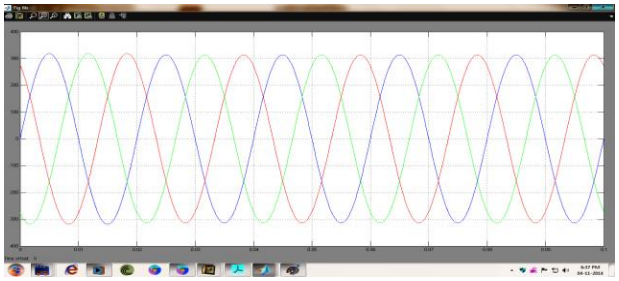

Fig. 5 (b) Source voltages.

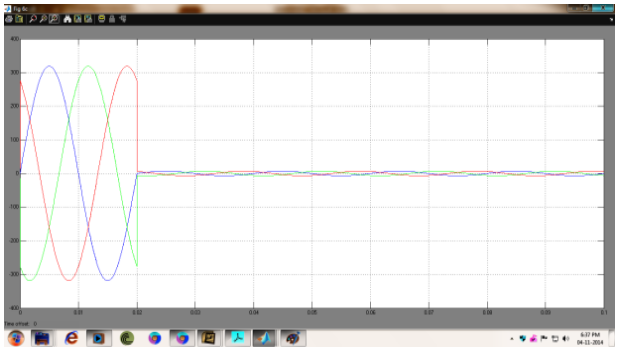

Fig. 5 (c) Load voltages.

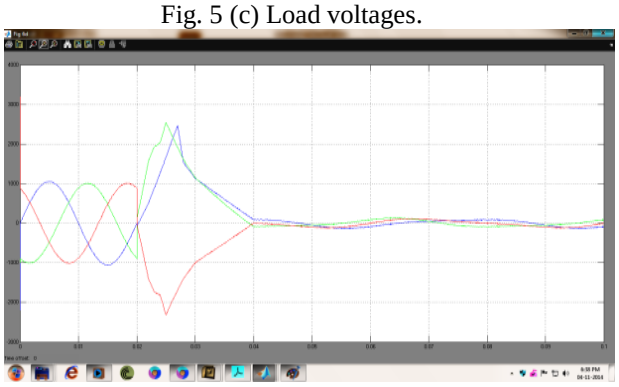

Fig. 5 (d) Line currents.

Fig.5 (e) DC-link voltage, during the three-phase downstream fault.

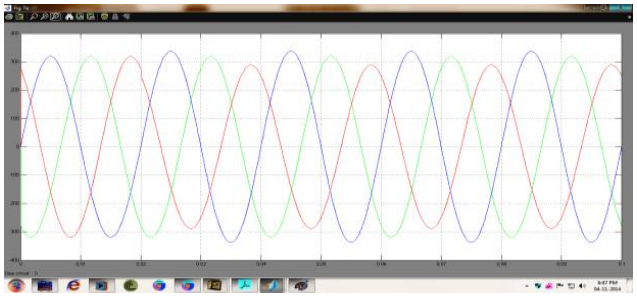
Fig. 6. (a) Voltages at bus3.


Fig.6 (b) Fault currents, during downstream phase-to-phase fault when the DVR is inactive (bypassed).

B. Phase-to-Phase Downstream Faults

The system of Fig. 3 is subjected to a phase-A to phase-C fault with the resistance of 0.05 Ω at 10% of the cable length connecting to bus4 and bus5, at 20ms. When the DVR is inactive (bypassed) during the fault, the PCC voltage drops to 0.88p.u, and the fault current increases to about 11 times the rated load current.

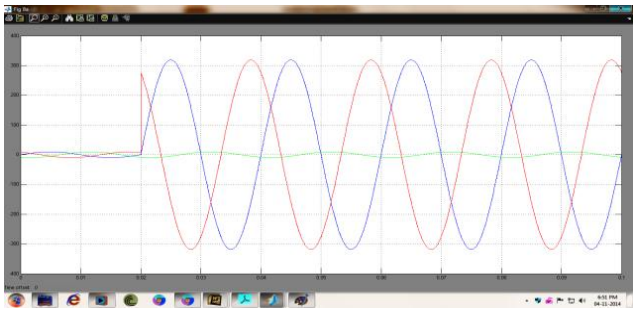
Fig.7 (a) Injected voltages

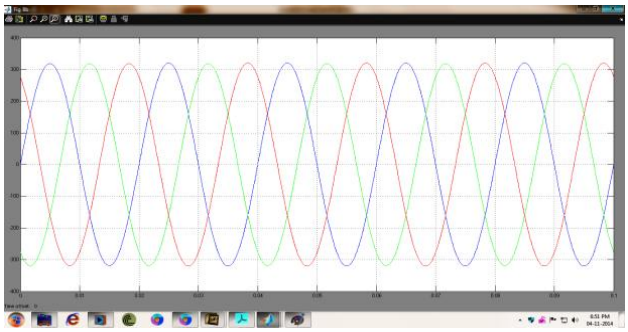
Fig. 7 (b) Source voltages.


Fig. 7 (c) Load voltages.

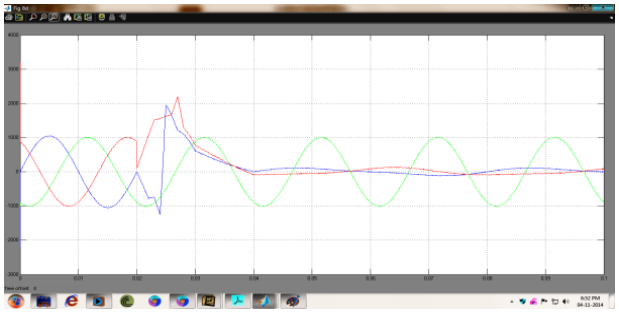
Fig. 7 (d) Line currents.

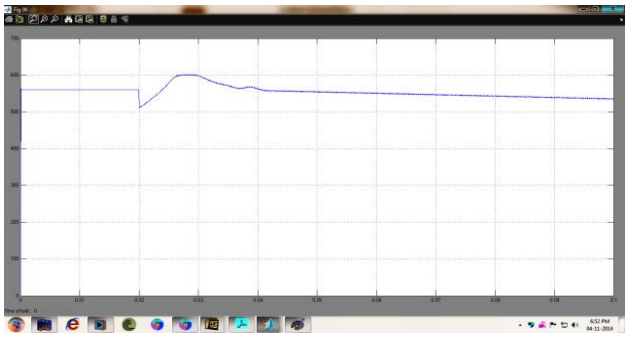
Fig. 7 (e) DC-link voltage, during the phase-to-phase downstream fault.

C. Single-Phase-to-Ground Downstream Fault

Phase-A of the system of Fig. 3 is subjected to a fault with the resistance of 0.2Ω at 10% length of the cable connecting to bus4 and bus5 , at 20ms. If the DVR is inactive, the PCC voltage does not considerably drop and the fault current is about 2.5p.u. It must be noted that although the PCC voltage drop is not considerable, the fault current must be interrupted by the DVR to prevent possible damages to the VSC before the fault is interrupted by the relays. The reason is that the operation time of the over current relays is considerable for a fault current of about 2.5p.u.

Fig. 8. (a) Voltages at bus3.

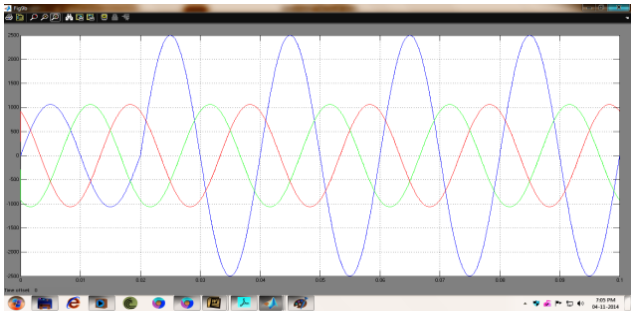

Fig.8 (b) Fault currents, during the downstream single-phase to-ground fault when the DVR is inactive (bypassed).

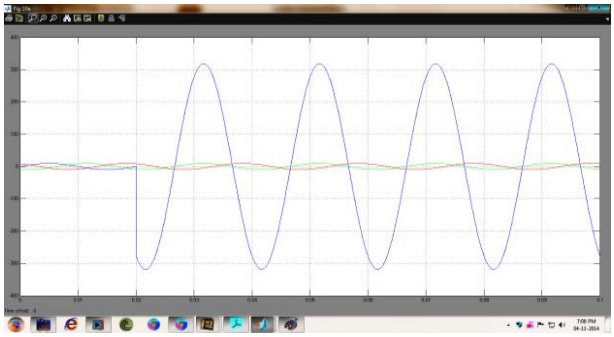

Fig.9 (a) Injected voltages.

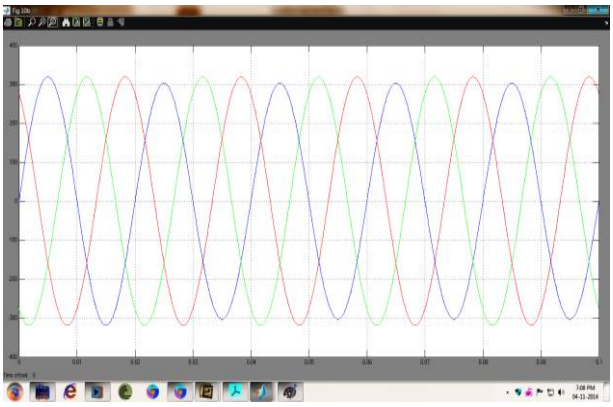

Fig.9 (b) Source voltages.

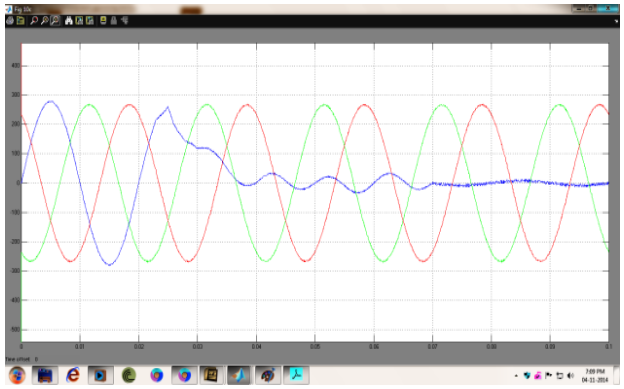

Fig. 9 (c) Load voltages.

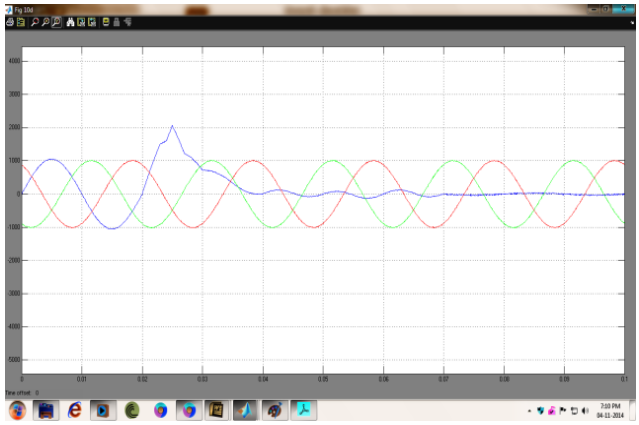

Fig. 9 (d) Line currents.

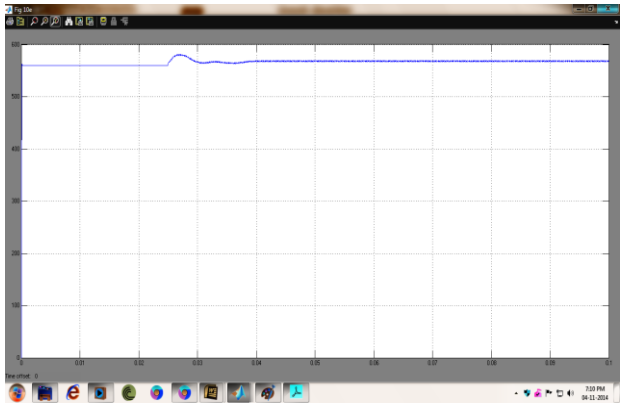

Fig. 9 (e) DC-link voltage, during the single-phase-to-ground downstream
Fault:

D. Simultaneous FCI Operation and Sag Compensation

The proposed DVR control system performs two different functions (i.e., sag compensation and FCI). Thus, the mutual effects of these modes on each other must be evaluated. At 15 ms, the system of Fig. 3 is subjected to a phase-A to phase-B fault with the resistance of 1 at 90% of the line length from. The fault causes 87% voltage sag at the PCC. At 55 ms, another fault with the resistance of 0.2 on

phase-A at 10% length of the cable connecting to occurs.

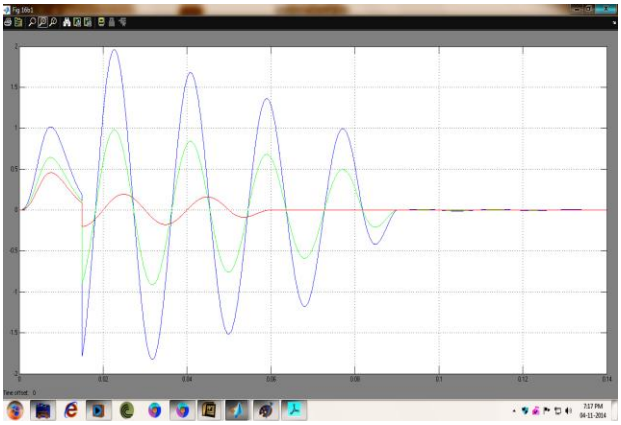

Fig. 16 (a) Line current of phase-A

Fig.16 (b) dc-link voltage, for different initial values of the dc-link voltage, during downstream phase-A-to-ground fault.

IV. CONCLUSION

This paper introduces an auxiliary control mechanism to enable the DVR to interrupt downstream fault currents in a radial distribution feeder. This control function is an addition to the voltage-sag compensation control of the DVR. The performance of the proposed controller, under different fault scenarios, including arcing fault conditions, is investigated based on time-domain simulation studies in the PSCAD/EMTDC environment. The study results conclude that:

1) The proposed multi loop control system provides a desirable transient response and steady-state performance and effectively damps the potential resonant oscillations caused by the DVR LC harmonic filter;

2) The proposed control system detects and effectively interrupts the various downstream fault currents within two cycles (of 50 Hz);

3) The proposed fault current interruption strategy limits the DVR dc-link voltage rise, caused by active power absorption, to less than 15% and enables the DVR to restore the PCC voltage without interruption; in addition, it interrupts the downstream fault currents even under low dc-link voltage conditions.

4) The proposed control system also performs satisfactorily under downstream arcing fault conditions

REFERENCES

[1] N. G. Hingorani, "Introducing custom power," *IEEE Spectr.*, vol. 32, no. 6, pp. 41–48, Jun. 1995.

[2] J. G. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," in *Proc. IEEE APEC'*, 2001, pp. 1267–1273.

[3] G. J. Li, X. P. Zhang, S. S. Choi, T. T. Lie, and Y. Z. Sun, "Control strategy for dynamic voltage restorers to achieve minimum power injection without introducing sudden phase shift," *Inst. Eng. Technol. Gen. Transm. Distrib.*, vol. 1, no. 5, pp. 847–853, 2007.

[4] S. S. Choi, B. H. Li, and D. M. Vilathgamuwa, "Design and analysis of the inverter-side filter used in the dynamic voltage restorer," *IEEE Trans. Power Del.*, vol. 17, no. 3, pp. 857–864, Jul. 2002.

[5] B. H. Li, S. S. Choi, and D. M. Vilathgamuwa, "Design considerations on the line-side filter used in the dynamic voltage restorer," *Proc. Inst. Elect. Eng., Gen. Transm. Distrib.*, vol. 148, no. 1, pp. 1–7, Jan. 2001.

[6] S. S. Choi, B. H. Li, and D. M. Vilathgamuwa, "Dynamic voltage restoration with minimumenergy injection," *IEEE Trans. Power. Syst.*, vol. 15, no. 1, pp. 51–57, Feb. 2000.

[7] Y. W. Li, D.M. Vilathgamuwa, P. C. Loh, and F. Blaabjerg, "A dualfunctional medium voltage level DVR to limit downstream fault currents," *IEEE Trans. Power. Electron.*, vol. 22, no. 4, pp. 1330–1340, Jul. 2007.

[8] Y. W. Li, D. M. Vilathgamuwa, F. Blaabjerg, and P. C. Loh, "A Robust control scheme for medium-voltage-level DVR implementation," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2249–2261, Aug. 2007.

[9] S. S. Choi, T. X. Wang, and D. M. Vilathgamuwa, "A series compensator with fault current limiting function," *IEEE Trans. Power Del.*, vol. 20, no. 3, pp. 2248–2256, Jul. 2005.

[10] B. Delfino, F. Fornari, and R. Procopio, "An effective SSC control scheme for voltage sag compensation," *IEEE Trans. Power Del.*, vol. 20, no. 3, pp. 2100–2107, Jul. 2005.

[11] C. Zhan, V. K. Ramachandaramurthy, A. Arulampalam, C. Fitzer, S. Kromlidis, M. Barnes, and N. Jenkins, "Dynamic voltage restorer based on voltage-space-vector PWM control," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1855–1863, Nov./Dec. 2001.
[12] D. M. Vilathgamuwa, P. C. Loh, and Y. Li, "Protection of microgrids during utility voltage sags," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1427–1436, Oct. 2006.
[13] F. Badrkhani Ajaei, S. Afsharnia, A. Kahrobaeian, and S. Farhangi, "A fast and effective control scheme for the dynamic voltage restorer," *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2398–2406, Oct. 2011.
[14] M. S. Sachdev and M. A. Barlbeau, "A new algorithm for digital impedance relays," *IEEE Trans. Power App., Syst.*, vol. PAS-98, no. 6, pp. 2232–2240, Nov./Dec. 1979.
[15] S. R. Naidu and D. A. Fernandes, "Dynamic voltage restorer based on a four-leg voltage source converter," *Inst. Eng. Technol. Gen. Transm. Distrib.*, vol. 3, no. 5, pp. 437–447.

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